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QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	09/897,158	Prepared by	NH	Tracking Number	05903949
Examiner-GAU	Wille - 2814	Date	3-17-4	Week Date	02/16/04
		No. of queries	2	IFW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE

① Claims 3-4 (originally claims 7 and 8, respectively) depends on claim 7 (originally claim 6. Please Advise and correct claim dependency.

② Claim 6 (now claim 7) depends on claim 11. Please Advise and correct claim dependency.

Thankyou

initials NH

RESPONSE

Index corrected.

CLM PTO supplied (best available copy) with claims & dependencies renumbered according to index.

initials JBH

E-5 (Rev. 10/01/02)

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION			
O.I.P.E. CLASSIFIER		15	
FORMALITY REVIEW	cy	1122	08/21/01
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✔	Rejected	N	Non-elected
=	Allowed	I	Interference
–	(Through numeral)... Canceled	A	Appeal
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If more than 150 claims or 10 actions staple additional sheet here

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1/1 (Amended) A method of creating a hybridized chip combining a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

attaching a carrier to the top active optical device;

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

2 (Amended) The method of claim 1 further comprising:

removing the carrier after the connecting.

5 (Amended) The method of claim 1, 2, 3 or 4 wherein the connecting comprises:

patterning traces between the points and the locations correspondingly aligned with the at least some electronic chip contacts, and

making the traces electrically conductive.

6 7. (Amended) The method of claim 5 wherein the patterning traces comprises:

patterning at least some of the traces on the substrate and at least some other of the traces on the electronic chip.

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7 8. (Amended) The method of claim 5 wherein the patterning traces further comprises:

patterning traces on the electronic chip.

5 9 10 (Amended) A method of creating a hybridized chip combining a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

thinning the substrate;

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

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~~10~~ (Amended) A method of creating a hybridized chip combining a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device;

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

~~14~~ 14. The method of claim ~~10~~ 13 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

17 (Amended) A hybridized chip comprising:

at least one top active optical device coupled to an electronic chip, the hybridized chip having been created using the method of one of claims 1-16.

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~~20~~ The method of claim ~~2~~ 1 further comprising:

thinning the substrate.

~~19~~ 4

~~21~~ The method of claim ~~2~~ 1 further comprising:

thinning the substrate.

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8 22. The method of claim 1, 2, 3, 4, 5, 20 or 21 further comprising attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device.

9 23. The method of claim 8 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

Amend

11 24. The method of claim 10 further comprising attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device.

12 25. The method of claim 11 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

15 26. The method of claim 1, 2, 10, 13, 14, 3, 4, 11 12 wherein the making the sidewalls electrically conductive comprises:

filling at least some of the openings with an electrically conductive material.

16 27. The method of claim 1, 2, 10, 13, 14, 3, 4, 11 12 wherein the making the sidewalls electrically conductive comprises:

depositing an electrically conductive material on at least some of the sidewalls.--